Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for issuing instructions in a multithreaded computer processor, the method comprising the steps of:

receiving a set of computer instructions in an instruction issue logic, wherein each instruction of said set comprises one instruction from each of a plurality of independent instruction threads;

identifying as dependent instructions those received instructions that require a result from a prerequisite instruction;

determining a probability for each received instruction that the instruction will complete all stages of a multi-stage instruction pipeline of the processor without causing a stall, wherein the probability for each received instruction is expressed as a percentage value;

selecting the received instruction of the set that is least likely to cause a stall in the multi-stage pipeline; and

issuing the selected instruction into the pipeline for processing, from the instruction issue logic, when the probability for the selected instruction is above a predetermined threshold that is 50%.

2. (Currently Amended) The method of claim 1, further comprising the step[[s]] of: determining whether there is a shared resource conflict between two or more of the received instructions of the set.

3. (Previously Presented) The method of claim 2, further comprising the step of:
resolving a given one of said shared resource conflicts between two or more of said received instructions, after said given conflict has been discovered.

4. (Cancelled)

5. (Previously Presented) The method of claim 1, further comprising:

predicting a stage, within the multi-stage instruction pipeline, where results of each instruction will be available, and said step of determining the probability for a received instruction includes calculating a critical distance comprising the number of stages between a stage when the instruction will need a given result, and the stage when the result will be available.

6. (Previously Presented) The method of claim 5, wherein the probability for a dependent instruction is determined based upon the current location and the predicted stage of any prerequisite instruction and upon a predicted resolution of any identified shared resource conflict.

7. (Previously Presented) The method of claim 6, further comprising the step of:

dynamically recalculating the probability for each instruction based on the current contents of the pipeline and a current status of any shared resources.

8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Currently Amended) A simultaneous multithreaded computer processor with speculative instruction issue that increases throughput, the computer processor comprising:

multiple independent input buffers, wherein one set of buffers is provided for each of a plurality of independent threads of instructions;

instruction issue logic that has an output buffer and is connected to the independent input buffers, wherein the instruction issue logic:

receives a set of instructions comprising one instruction from each of the threads of instructions;

identifies as dependent instructions those received instructions that require a result from a prerequisite instruction;

determines a probability for each instruction that the instruction will complete all stages of a multi-stage instruction pipeline of the processor without causing a stall, wherein the probability for each received instruction is expressed as a percentage value;

selects the received instruction of the set that is least likely to cause a stall in the multi-stage pipeline; and

issues the selected instruction into the pipeline for processing, from the instruction issue logic, when the probability for the selected instruction is above a predetermined threshold that is 50%; and

wherein a first stage of the multi-stage pipeline is connected to an output buffer of the instruction issue logic.

17. (Previously Presented) The computer processor of claim 16, wherein the instruction issue logic determines whether there is a shared resource conflict between two or more of the received instructions.

18. (Previously Presented) The computer processor of claim 16, wherein the instruction issue logic resolves a given one of said shared resource conflicts, between two or more of said received instructions, after said given conflict has been discovered.

19. (Cancelled)

20. (Previously Presented) The computer processor of claim 16, wherein the instruction issue logic predicts a stage, within the multi-stage instruction pipeline, where results of each instruction will be available, and determines the probability for a dependent instruction by calculating a critical distance comprising the number of stages between a stage when the dependent instruction will need a given result, and the stage when the result will be available.

21. (Original) The computer processor of claim 16, wherein the instruction issue logic further identifies as dependent instructions those received instructions that have a conflict over a shared resource within a computer system in which the computer processor operates.

22. (Previously Presented) The computer processor of claim 21, wherein the probability for a dependent instruction is determined based upon a current location and the predicted stage of any prerequisite instruction and upon a predicted resolution of any identified shared resource conflict.

23. (Currently Amended) The computer processor of claim[[s]] 22, wherein the instruction issue logic dynamically recalculates the probability for each instruction based on current contents of the pipeline and a current status of any shared resources.

24. (Cancelled)

25. (Cancelled)

26. (Cancelled)

27. (Cancelled)

28. (Cancelled)

29. (Cancelled)

30. (Cancelled)

31. (Currently Amended) A method for issuing instructions in a multithreaded computer processor, comprising the steps of:

receiving a set of computer instructions in an instruction issue logic, wherein each set of instructions comprises one instruction from each of a plurality of independent instruction threads;

predicting a stage, within a multi-stage instruction pipeline of the computer processor, where results of each instruction will be available;

identifying as dependent instructions those received instructions that require a result from a prerequisite instruction;

calculating a critical distance comprising the number of stages between a stage when a selected dependent instruction will need a given result, and the stage when the result will be available;

determining whether the selected instruction is within the critical distance, and if so, determining a probability that the selected instruction will complete all stages of the pipeline without causing a stall, wherein said probability is expressed as a percentage value; and,

issuing the selected instruction into the pipeline for processing, from the instruction issue logic, when the probability is above a predetermined threshold that is 50%.

32. (Cancelled)

33. (Cancelled)

34. (Currently Amended) A computer program product in a computer readable medium for issuing instructions in a multithreaded computer processor, wherein the computer program product comprises:

first instructions for receiving a set of computer instructions in an instruction issue logic, wherein each instruction of said set comprises one instruction from each of a plurality of independent instruction threads;

second instructions for identifying as dependent instructions those received instructions that require a result from a prerequisite instruction;

third instructions for determining a probability for each received instruction that the received instruction will complete all stages of the processor without causing a stall, wherein the probability for each received instruction is expressed as a percentage value;

fourth instructions for selecting the received instruction of the set that is least likely to cause a stall in the multi-stage pipeline; and

fifth instructions for issuing the selected instruction into the pipeline for processing, from the instruction issue logic, when the probability for the selected instruction is above a predetermined threshold that is 50%.

35. (Previously Presented) The computer program product of claim 34, further comprising:

sixth instructions for determining whether there is a shared resource conflict between two or more of the received instructions of said set.

36. (Previously Presented) The computer program product of claim 35, wherein a given one of said shared resource conflicts, between two or more of said received instructions, is resolved after said given conflict has been discovered.

37. (Cancelled)

38. (Previously Presented) The computer program product of claim 34, further comprising:

seventh instructions for predicting a stage, within the multi-stage instruction pipeline, where results of each instruction will be available, and determining a probability for a received instruction by

calculating a critical distance comprising the number of stages between a stage when the instruction will need a given result, and the stage when the result will be available.

39. (Previously Presented) The computer program product of claim 38, wherein the probability for a dependent instruction is determined based upon the current location and the predicted stage of any prerequisite instruction and upon a predicted resolution of any identified shared resource conflict.

40. (Previously Presented) The computer program product of claim 39, wherein the probability for each instruction is dynamically recalculated, based on the current contents of the pipeline and a current status of any shared resources.